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AN/"POLAR SEMICONDUCTOR": 29 patents.
*Hits **1** through **29** out of **29***

Jump To

Refine Search AN/"POLAR SEMICONDUCTOR"

	PAT. NO.	Title
1	10,580,861	Trench semiconductor device layout configurations
2	10,388,783	Floating-shield triple-gate MOSFET
3	10,332,992	Semiconductor device having improved trench, source and gate electrode structures
4	10,153,366	LDMOS transistor with lightly-doped annular RESURF periphery
5	10,141,440	Drift-region field control of an LDMOS transistor using biased shallow-trench field plates
6	9,899,343	High voltage tolerant bonding pad structure for trench-based semiconductor devices
7	9,818,828	Termination trench structures for high-voltage split-gate MOS devices
8	9,818,742	Semiconductor device isolation using an aligned diffusion and polysilicon field plate
9	9,704,765	Method of controlling etch-pattern density and device made using such method
10	9,269,705	Anti-snapback circuitry for metal oxide semiconductor (MOS) transistor
11	8,994,152	Metal shield for integrated circuits
12	8,891,262	Series switch bridgeless power supply
13	8,564,155	Multiple output power supply
14	8,476,879	Saving energy mode (SEM) for an interleaved power factor correction (PFC) converter
15	8,461,661	Locos nitride capping of deep trench polysilicon fill
16	8,427,069	Current-regulated power supply with soft-start protection
17	8,385,029	Over-current protection device for a switched-mode power supply
18	8,248,041	Frequency compression for an interleaved power factor correction (PFC) converter
19	8,248,040	Time-limiting mode (TLM) for an interleaved power factor correction (PFC) converter
20	8,085,563	Protection and clamp circuit for power factor correction controller
21	8,044,699	Differential high voltage level shifter
22	8,000,073	Current-mode under voltage lockout circuit
23	7,915,129	Method of fabricating high-voltage metal oxide semiconductor transistor devices
24	7,817,391	Over-current protection device for a switched-mode power supply
25	7,466,004	Diode structure to suppress parasitic current
26	7,185,302	Method for generating layouts by chamfering corners of polygons

27 7,135,750 T Photodiode array having reduced dead space
28 7,071,533 T Bipolar junction transistor antifuse
29 7,043,711 T System and method for defining semiconductor device layout parameters

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Top View Cart
Home Quick Advanced Pat Num Help