
Related U.S. Patent Documents

<u>Application Number</u>	<u>Filing Date</u>	<u>Patent Number</u>	<u>Issue Date</u>
62192800	Jul 15, 2015		

Current U.S. Class: 1/1

Current CPC Class: H01B 1/22 (20130101); H05K 3/4691 (20130101); H05K 1/0281 (20130101); H05K 3/429 (20130101); H05K 2201/09063 (20130101); H05K 2201/09563 (20130101); H05K 2201/09518 (20130101)

Current International Class: H05K 3/42 (20060101); H01B 1/22 (20060101); H05K 3/46 (20060101); H05K 1/02 (20060101)

References Cited [\[Referenced By\]](#)

U.S. Patent Documents

5504277	April 1996	Danner
6485827	November 2002	Griffith et al.
9545017	January 2017	Hunrath
2001/0009273	July 2001	John
2002/0040522	April 2002	Ohya et al.
2008/0296052	December 2008	Inagaki
2009/0056987	March 2009	Nomiya
2011/0073358	March 2011	Hayashi
2011/0099806	May 2011	Koyama
2013/0043067	February 2013	Hayashi
2013/0153279	June 2013	Hayashi
2014/0231126	August 2014	Hunrath
2015/0060124	March 2015	Terui
2015/0060127	March 2015	Terui

Other References

International Patent Application No. PCT/US16/42359, Notification of Transmittal of the International Search Report and The Written Opinion of the International Searching Authority, of the Declaration, dated Sep. 26, 2016, 13 pages. cited by applicant .
 First Office Action for corresponding Chinese Patent Application No. 201680051216.8 dated Mar. 13, 2019, 12 pages. cited by applicant.

Primary Examiner: Arbes; Carl J

Attorney, Agent or Firm: Morgan, Lewis & Bockius LLP

Parent Case Text

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a U.S. National Phase Application under 35 U.S.C. 371 of International Application No. PCT/US2016/042359 filed Jul. 14, 2016, which claims the benefit of U.S. Provisional Patent Application No. 62/192,800 filed Jul. 15, 2015 entitled "Methods of Manufacturing printed Circuit Boards", all of which are incorporated by reference herein in their entireties.

Claims

What is claimed is:

1. A process for fabricating printed circuit boards, comprising the steps of: providing a laminated printed circuit board subassembly having a top surface and a plurality of vias; each of the plurality of vias including a top surface opening in the top surface; applying a polymer film to the top surface of the laminated printed circuit board subassembly; creating a hole in the polymer film proximate each of a plurality of top surface openings so as to expose the top surface opening of each of the plurality of vias to facilitate access to each of the plurality of vias for a subsequent hole-fill step, wherein creating the hole in the polymer film proximate the plurality of top surface openings further comprises: using a computer numeric controlled laser to cut the polymer film in a manner directed by a computer program to expose the plurality of top surface openings; and filling each of the plurality of vias with hole-fill paste.
2. The process of claim 1, wherein the polymer film is an adhesive backed polymer film having an adhesive backing; and wherein the step of applying the adhesive backed polymer film to the top surface includes adhering the adhesive backing to the top surface.
3. The process of claim 1, wherein the step of applying the polymer film to the top surface further includes the step of applying an adhesive to a back surface of the polymer film such that the adhesive adheres to the back surface of the polymer film; and the step of applying the polymer film to the top surface of the laminated printed circuit board subassembly includes adhering the adhesive to the top surface.
4. The process of claim 1, wherein the hole-fill paste is a hole-fill paste that will at least partially harden when it is cured, and wherein, after filling each of the plurality of vias with hole-fill paste, the process further including the step of at least partially curing the hole-fill paste.
5. The process of claim 4, wherein, after the step of at least partially curing the hole-fill paste, the process further including the step of: removing the polymer film from the top surface of the laminated printed circuit board subassembly.
6. The process of claim 5, wherein the step of at least partially curing the hole-fill paste includes curing the hole-fill paste at a curing time period between two hours and four hours.
7. The process of claim 6, wherein the step of at least partially curing the hole-fill paste includes curing the hole-fill paste for a time selected from: between 1 and 48 hours, between 1 and 36 hours, between 1 and 24 hours, between 1 and 12 hours, between 1 and 6 hours, between 1 and 5 hours, between 1 and 4 hours, and between 2 and 4 hours.
8. The process of claim 6, wherein the step of at least partially curing the hole-fill paste includes curing the hole-fill paste for a time selected from: about 1 hour, about 2 hours, about 3 hours, about 4 hours, about 5 hours, about 6 hours, about 7 hours, about 8 hours, about 9 hours, about 10 hours, about 11 hours, about 12 hours, about 13 hours, about 14 hours, about 15 hours, about 16 hours, about 17 hours, about 18 hours, about 19 hours, about 20 hours, about 21 hours, about 22 hours, about 23 hours, about 24 hours, about 25 hours, about 26 hours, about 27 hours, about 28 hours, about 29 hours, about 30 hours, about 31 hours, about 32 hours, about 33 hours,

32. A process for fabricating printed circuit boards, comprising the steps of: providing a laminated printed circuit board subassembly having a top surface, a bottom surface and a plurality of vias; each of the plurality of vias including a top surface opening in the top surface and a bottom surface opening in the bottom surface; applying a first sheet of polymer film to the top surface of the laminated printed circuit board subassembly and a second sheet of polymer film to the bottom surface of the laminated printed circuit board subassembly; and creating a plurality of holes in each of the respective sheets of polymer film, each of which is proximate one of the plurality of top surface openings or the plurality of bottom surface openings, respectively, so as to expose each of the respective openings to facilitate a subsequent step of filling each of the vias with hole-fill paste, wherein creating the plurality of holes in each of the respective sheets of polymer film proximate the plurality of openings in the top surface and the bottom surface, respectively, further comprises: using a computer numeric controlled laser to cut the polymer film in a manner directed by a computer program to expose the plurality of top and bottom surface openings.

Description

BACKGROUND

Field of the Invention

The present invention pertains generally to rigid, flexible, and rigid flex printed electronic circuit boards (referred to herein as "printed circuit boards"), particularly, laminated assemblies of printed circuit boards, having vias and/or through holes and methods of manufacturing the same. More particularly, the invention relates to methods of protecting laminated printed circuit boards during hole-fill operations, methods-of manufacturing products according to such methods, and products made according to such methods.

Description of the Prior Art

In the art of fabricating printed circuit boards, such circuits are often laminations with a plurality of circuit layers. To connect selected portions of the circuits on two or more layers, holes can be created in each of these layers. When the layers are aligned and processed to form a laminated structure, the aligned holes are plated with conductor and/or filled with conductive paste, so that the holes provide an electrical pathway or via to electrically connect the layers.

A via used for electrical communication between conductive path layers of the printed circuit board typically has conductive pads in corresponding positions on a plurality of layers of the printed circuit board that are connected by a hole through the board. The hole is typically made conductive by electroplating. Vias may extend all the way through the printed circuit board, with a top surface opening in the top surface of the printed circuit board, and an adjacent pad on the top surface, and bottom surface opening in the bottom surface of the printed circuit board, and an adjacent pad on the bottom surface, for example. Alternatively, vias can extend through some, but not all, of the layers of the printed circuit board. For example, some vias that extend through some of the layers of the printed circuit board, but are exposed only on the top surface or the bottom surface of the printed circuit board, but not both, are called blind vias. Vias which extend through some of the layers of the printed circuit board, but are not exposed on either the, top surface or the bottom surface of the printed circuit board, are called buried vias. Such vias typically comprise a barrel portion (i.e., a conductive tube that fills a drilled hole), pads that connect each end of the barrel to a component, a layer, or a trace, and often one or more antipads that provide clearance gaps between the barrel and a metal layer so that the layer or trace is not connected. A via may be proximate the edge of the board so that it is cut in half when the board is separated. This is known as a castellated hole and is used for a variety of reasons, including allowing one printed circuit board to be soldered to another in a stack. Some vias are used for heat transfer and are called thermal vias and are typically used to carry heat away from power devices and are typically used in arrays of multiple vias.

FIG. 5 is a schematic cross-sectional view illustrating hole-fill paste applied to the laminated circuit board subassembly of FIG. 4D;

FIG. 6 is a schematic cross-sectional view illustrating the laminated circuit board subassembly of FIG. 5 after removal of the polymer film;

FIG. 7 is a schematic cross-sectional view illustrating the laminated circuit board subassembly of FIG. 6 after removal of excess hole-fill paste;

FIG. 8 is a schematic cross-sectional view illustrating the laminated circuit board subassembly of FIG. 7 after applying a conductive overcoat;

FIG. 9 is a schematic cross-sectional view illustrating the laminated circuit board subassembly of FIG. 8 after applying solder;

FIG. 10 is a schematic cross-sectional view of a rigid board for reinforcing a portion of the laminated circuit board subassembly of FIG. 9;

FIG. 11 is a schematic cross-sectional view illustrating the rigid board of FIG. 10 attached to a portion of the laminated circuit board subassembly of FIG. 9;

FIG. 12 is an isometric view illustrating a printed circuit board comprising the laminated circuit board subassembly of FIG. 11 populated with surface-mounted component(s);

FIG. 13 is a flow diagram illustrating an example process embodiment of the present invention; and

FIG. 14 is a flow diagram illustrating a further example process embodiment of the present invention.

DETAILED DESCRIPTION

The fabrication of printed circuit boards, flexible electronic circuits, and rigid flex circuits has developed to great success, with many methods and refinements over the years, but still with limitations and difficulties in some situations. The present invention addresses limitations and difficulties in fabricating certain types of such circuit boards, especially including rigid flex circuit boards. As referenced herein, the terminology "printed circuit boards" (or "PCB") is meant to include similar flexible electronic circuit boards and rigid flex circuit boards. Such printed circuit boards are typically fabricated by laminating multiple conductive and nonconductive layers, with precisely patterned conductive layers fabricated by photochemical etching processes, printing-type processes, or other additive or subtractive processes.

Although a printed circuit board can have a single base layer, with a conductive patterned layer printed on one or both side of the base layer, a laminated printed circuit subassembly is typically formed of a plurality of layers, each layer being a subassembly having a nonconductive base layer and a conductive patterned layer printed on one or both sides of the base layer, providing conductive paths between various areas of the subassembly. Each subassembly also has various holes, and may have cut-outs through the layer. The plurality of subassemblies are stacked together in alignment and laminated, with some of the holes and cut-outs aligning between a plurality of layers, or completely through the entire laminated printed circuit board subassembly. One or more insulating layers or portions of layers may be included in the laminated printed circuit board subassembly, to limit electrical conduction between adjacent layer subassemblies. One or more dielectric layers, or portions of layers, may be included in the laminated printed circuit board subassembly, to provide capacitance. One or more rigid layers or "boards", or portions of layers, may be included in the laminated printed circuit board subassembly, to provide rigidity, support, or strength. Where it is desired to conduct between a plurality of subassemblies or layers at locations of holes, a conductive hole plating is applied to the hole. The plated hole then acts as a "via" to conduct electricity between the subassemblies or layers, specifically at the locations of the via. From the via, the various conductive pattern layers of each subassembly conduct electricity to selected areas of the

access holes 46 in the polymer film 40, 42 proximate the openings 28, 30 to the respective vias 18 or conductive vias 22 on the top and bottom surfaces 24, 26 of the covered laminated PCB subassembly 20B. The access holes 46 allow the manufacturer to fill the respective vias 18, 22 through the respective openings 28, 30 and the polymer film 40, 42 can prevent or at least minimize the degree to which the hole-paste will migrate to other areas on the respective surfaces of the covered laminate PCB subassembly 20B, so that other areas are masked and protected by polymer film 40, 42. In preferred embodiments, a covered laminate PCB subassembly 20' is created where the adhesive backing on the polymer film 40, 42 adheres edges of the respective holes 46 to the respective surface 24, 26 so that hole-fill paste 50 is unable to migrate away from the respective openings 28, 30 along the respective surface 24, 26. A laser system for creating or cutting holes 46 may be computer-controlled, or a CNC laser system, with a computer program or software template corresponding to a desired cut pattern.

After applying polymer film 40, 42 the respective surface and creating holes 46 in the respective polymer film 40, 42 to permit access to selected locations, such as the respective openings 28, 30 to the respective vias 18, 22, hole-fill paste 50 is applied to the covered laminated PCB subassembly 20B in order to fill selected vias 18 and/or conductive vias 22 as desired. Hole-fill paste 50 is forced into vias 18 or conductive vias 22 so as to avoid significant air inclusions which can be detrimental, and the outer surface of the polymer film 40, 42 is typically wiped clean with a squeegee to remove excess hole-fill paste 50 that extends out beyond the polymer film 40, 42 proximate the respective access holes 46, to create a covered and filled laminated printed circuit board subassembly 20C such as that illustrated in FIG. 5.

Prior to removing polymer film 40, 42, the hole-fill paste 50 is preferably cured or hardened sufficiently to stabilize hole-fill paste 50 so that it will not break away from the areas proximate the respective openings 28, 30 during removal of polymer film 40, 42.

The amount of curing is based on the curing time and the curing temperature. In some embodiments, curing is conducted for a time selected from: between 1 and 48 hours, between 1 and 36 hours, between 1 and 24 hours, between 1 and 12 hours, between 1 and 6 hours, between 1 and 5 hours, between 1 and 4 hours, and between 2 and 4 hours. In some embodiments, curing is conducted for a time selected from: about 1 hour, about 2 hours, about 3 hours, about 4 hours, about 5 hours, about 6 hours, about 7 hours, about 8 hours, about 9 hours, about 10 hours, about 11 hours, about 12 hours, about 13 hours, about 14 hours, about 15 hours, about 16 hours, about 17 hours, about 18 hours, about 19 hours, about 20 hours, about 21 hours, about 22 hours, about 23 hours, about 24 hours, about 25 hours, about 26 hours, about 27 hours, about 28 hours, about 29 hours, about 30 hours, about 31 hours, about 32 hours, about 33 hours, about 34 hours, about 35 hours, about 36 hours, about 37 hours, about 38 hours, about 39 hours, about 40 hours, about 41 hours, about 42 hours, about 43 hours, about 44 hours, about 45 hours, about 46 hours, about 47 hours and about 48 hours.

In some embodiments, the curing is conducted at a temperature selected from: between 18.degree. C. (64.degree. F.) and 30.degree. C. (86.degree. F.), between 19.degree. C. (66.degree. F.) and 27.degree. C. (80.degree. F.), between 20.degree. C. (68.degree. F.) and 25.degree. C. (77.degree. F.), and between 21.degree. C. (70.degree. F.) and 23.degree. C. (73.degree. F.). In some embodiments, the curing is conducted at a temperature selected from: about 18.degree. C., about 19.degree. C., about 20.degree. C., about 21.degree. C., about 22.degree. C., about 23.degree. C., about 24.degree. C., about 25.degree. C., about 26.degree. C., about 27.degree. C., about 28.degree. C., about 29.degree. C., about 30.degree. C.

As used herein, the term "about" may refer to + or -10% of the value referenced. For example, "about 9" is understood to encompass 8.2 to 9.9.

In preferred embodiments, after "soft" or partial curing or after hardening of hole-fill paste 50 to ensure that hole-fill paste 50 stays in position as desired, the polymer film 40, 42 is removed from the covered and filled laminated printed circuit board subassembly 20', to form a filled laminated printed circuit board subassembly 200, such as that illustrated in FIG. 6. Typically, excess hole-fill paste 50 extending above the respective openings 28, 30 to the respective vias 18, 22 will be exposed after polymer film 40, 42 is removed, as illustrated in FIG. 6.

Typically, any such undesired hole-fill paste 50 extending above the respective openings 28, 30 to the respective vias 18, 22 will then be removed, such as by a local sanding or other machining operation, to leave the outer surface of the hole-fill paste 50 flush with the top of the conductive hole plating 32 proximate the respective opening 28, 30. This step will leave the surface of the hole-fill paste flat the respective openings 28, 30 on filled and leveled laminated printed circuit board subassembly 20E illustrated in FIG. 7. In preferred embodiments, the hole-fill paste 50 is then further cured or hardened to provide improved strength and stability. This curing or hardening may be a complete or "hard" curing beyond the "soft" curing or hardening as described above. Alternatively, the initial curing or hardening prior to removal of polymer film 40, 42 may provide sufficient strength and stability without a separate, second curing or hardening step.

As illustrated in FIG. 8, a conductive overcoat 80 may be applied such as by a "printing" or plating process such as those previously described, to produce surface conductive paths of sufficient quality on an overcoated laminated printed circuit board subassembly 20F after a completion of a hole-fill process. The conductive overcoat 80 may comprise conductive pads such as solder pads 82 to facilitate attachment of and electrical communication with surface-mounted electrical components 122 (see FIG. 12), as well as various conductive pathways which incorporate these conductive solder pads 82. The conductive overcoat 80 may also comprise conductive pathways which do not incorporate conductive solder pads 82.

Surface-mounted components 122 can be attached to one or more exposed surfaces of the overcoated laminated printed circuit board subassembly 20F. These surface-mounted components 122 may include resistors, capacitors, inductors, relays, switches, lamps, display components, diodes, transistors, integrated circuits, sensors, cables, wires, connectors, sockets, and other components as are known in the art. Surface-mounted components 122 are located at specific sites such as solder pads 82 on the exposed surface(s) of the overcoated laminated printed circuit board subassembly 20F. To facilitate incorporation of surface-mounted components 122 in the circuit by applying them to and electrically connecting them to the surface layer, small amounts of solder 90 can be applied at specific locations such as solder pads 82 where surface-mounted components 122 are to be connected. Commonly, solder 90 is applied for attachment and electrical communication between these solder pads 82 and surface-mounted electrical components 122 as illustrated in FIG. 9. Hole-fill paste 50 in any via 18 or conductive via 22 near the location of solder 90 helps to prevent migration of solder 90 into the via 18 or conductive via 22.

One or more rigid layers 100, or portions of layers, may be included in overcoated laminated printed circuit board subassembly 20F, to produce rigid, flexible, or combination rigid flex circuit boards, as desired. Rigid board 100, as illustrated in FIG. 10, may be utilized for rigid layers in an overcoated laminated printed circuit board subassembly 20F.

FIG. 11 illustrates an example overcoated laminated printed circuit board subassembly 20F that includes a rigid board 100. In the example of FIG. 11, rigid board 100 is applied to bottom surface 26 of the overcoated laminated printed circuit board subassembly 20F after conductive overcoat 80 has been applied. Alternatively, rigid board 100 may be included between layers of overcoated laminated printed circuit board subassembly 20F, or may be applied to top surface 24 or bottom surface 26 of the overcoated laminated circuit board subassembly 20F. A plurality of rigid boards 100 may be included, at one or more locations in the overcoated laminated printed circuit board subassembly 20F, such as at both the top surface 24 and the bottom surface 26, or at a plurality of locations between subassemblies 10, within the overcoated laminated printed circuit board subassembly 20F, or combinations thereof. For a rigid flex circuit board, typically only portion(s) of an overcoated laminated circuit board subassembly 20F will be reinforced by rigid board 100, such as areas where surface-mounted components 122 will be applied, although it may be advantageous to reinforce other areas of a rigid flex circuit board, such as to aid in subsequent assembly into a device incorporating the printed circuit board. Rigid board 100 may be included between subassemblies 10 within the overcoated laminated printed circuit board subassembly 20F, such as by the lamination step, or applied to the top surface 24 or the bottom surface 26 of the overcoated laminated printed circuit board subassembly 20F by lamination or adhesive, thermal, chemical, compression, vacuum, or other methods or combinations such as those cited for applying polymer film 40 to the overcoated laminated printed circuit board subassembly 20F, for example. Rigid board 100 can comprise patterned conductive layer(s), and can have holes or vias 18 or conductive vias 22; in this way,

- [Home](#)
- [Quick](#)
- [Advanced](#)
- [Pat Num](#)
- [Help](#)